B.TECH SEM – IV (2007 COURSE) (ELECTRONICS) :
SUMMER - 2018
SUBJECT: DIGITAL ELECTRONICS AND LOGIC DESIGN

Day : **Thursday** Time: **10.00 AM TO 01.00 PM**
Date : **07/06/2018** **S-2018-2622** Max. Marks : 80

N. B. :

1) **Q. No. 1**and **Q. No. 5** are **COMPULSORY**. Out of remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the **SEPARATE** answer books.
4) Draw neat and labeled diagram **WHEREVER** necessary.
5) Assume suitable data, if necessary.

SECTION – I

Q.1 **a)** Reduce the following function using K-map technique. **(05)**
$F(A,B,C,D) = \Sigma m(1,2,9,10,11,14,15)$

b) Using 2's complement perform the following: **(04)**
i) $(42)_{10}-(68)_{10}$
ii) $(25)_{10}-(16)_{10}$

c) Write a short note on ECL logic family **(05)**

Q.2 **a)** Explain the following codes and state its applications **(07)**
i) Excess-3 code
ii) Gray code

b) Perform the following conversions: **(06)**
i) $(85.63)_{10} = (?)_2$
ii) $(204)_{10} = (?)_8$
iii) $(0.122)_{10} - (?)_{16}$

Q.3 **a)** Compare Canonical and standard forms with the help of example. **(04)**

b) Implement the following function using Quine-Mcluskey method. **(09)**
$F(A,B,C,D) = \Sigma m(0,2,3,6,7,8,10,11,13)$

Q.4 **a)** With the help of neat diagram explain working of 2-input TTL NAND gate. **(07)**

b) Differentiate between TTL and CMOS Logic family. **(06)**

SECTION - II

Q.5 **a)** Design a 1-bit magnitude comparator. **(05)**

b) Compare Decoder & Demultiplexer. **(04)**

c) What is meant by "Universal shift register"? **(05)**

Q.6 **a)** Design a 4-bit Binary to Gray code converter and implement it using basic logic gates. **(07)**

b) Design a full subtractor and explain it with the help of logic diagram. **(06)**

Q.7 **a)** Implement given multiple output function using a suitable decoder. **(07)**
$F_1(A,B,C,) = \Sigma m(0,4,7) + d(2,3)$
$F_2(A,B,C,) = \Sigma m(1,5,6)$
$F_3(A,B,C,) = \Sigma m(0,2,4,6)$

b) Explain with diagram the working of 1:16 demultiplexer. **(06)**

Q.8 **a)** Explain serial-in-parallel out shift register mode operation using IC7495. **(06)**

b) Design a MOD-5 ripple counter using a suitable flip flop. **(07)**

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