

**B. TECH. SEM -III (E & TC ENGG.) (2014 COURSE) (CBCS) :**  
**SUMMER - 2018**

**SUBJECT: DIGITAL CIRCUITS &APPLICATIONS**

Day: **Thursday**  
Date: **24/05/2018**

**S-2018-2268**

Time: **02.30 PM TO 05.30 PM**  
Max Marks. 60

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**N.B.**

- 1) All questions are **COMPULSORY**.
  - 2) Figures to the right indicate **FULL** marks.
  - 3) Use of non – programmable calculator is **ALLOWED**.
  - 4) Assume suitable data, if necessary.
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- Q.1 a)** Convert Binary numbers 1001011, 10110 to Grey code. **(05)**  
**b)** State and prove Demorgan's theorem. **(05)**

**OR**

- Q.1 a)** Convert the following decimal number to excess – 3 code **(05)**  
i) 430  
ii) 46  
**b)** Minimize the following Boolean functions **(05)**  
 $f(A,B,C,D) = \sum m ( 5,7,8,10,13,15) + \sum d ( 0,1,2,3)$

- Q.2 a)** What is multiplex? Explain 4:1 multiplexer. **(05)**  
**b)** Explain 1 – bit magnitude comparator. **(05)**

**OR**

- Q.2 a)** Draw the circuit of BCD – adder and explain its working. **(05)**  
**b)** What is priority encoder? **(05)**

- Q.3 a)** Explain CMOS inverter. **(05)**  
**b)** Define characteristics of digital ICs. **(05)**

**OR**

- Q.3 a)** What is ECL and explain it with neat circuit diagram. **(05)**  
**b)** Differentiate between totem – pole and open collector output stage **(05)**

- Q.4 a)** What is S-R flip - flop? Explain it with excitation table and neat diagram. **(05)**  
**b)** Differentiate between combinational circuit and sequential circuit. **(05)**

**OR**

- Q.4 a)** How is the race around condition eliminated using the flip - flop? **(05)**  
**b)** What is the difference between Mealy and Moore state machines? **(05)**

**P.T.O**

- Q.5** a) What is universal shift register? (05)  
b) Design MOD – 6 ripple counter. (05)

**OR**

- Q.5** a) Differentiate between Synchronous and Asynchronous counter. (05)  
b) Explain 3 – bit Up - down counter. (05)

- Q.6** a) Describe memory classification. (05)  
b) What is Programmable Logic Array? (05)

**OR**

- Q.6** a) Explain basic construction of binary cell (05)  
b) Explain MOSFET RAM cell (05)

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