M. TECH.-III (ELECTRONICS V.L.S.I.) (CBCS – 2015 COURSE) : SUMMER - 2018

SUBJECT: ELECTIVE –I ALGORITHMS FOR VLSI DESIGN AUTOMATION

Day : **Tuesday** **S-2018-3074** Time: **11.00 AM TO 02.00 PM**
Date : **29/05/2018** Max. Marks. : 60

N.B.:

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Answer to the both the sections should be written in **SEPARATE** answer books.
4) Assume suitable data if necessary.

SECTION-I

Q.1 Describe physical design cycle for VLSI design. **(10)**

OR

Q.1 Explain Depth First Search algorithm using suitable example. **(10)**

Q.2 What are the limitations of KL algorithm? How to overcome them? **(10)**

OR

Q.2 Explain the Simulated Annealing algorithm for partitioning. **(10)**

Q.3 Discuss Simulated Annealing and Timber Wolf algorithms for placement. **(10)**

OR

Q.3 Explain Breuer's algorithm for placement. **(10)**

SECTION-II

Q.4 Explain any two Steiner Tree based algorithm for global routing. **(10)**

OR

Q.4 Describe inter programming technique for routing. **(10)**

Q.5 Explain the classification of two layer algorithms for routing. Also discuss basic left edge algorithm. **(10)**

OR

Q.5 Describe Net Merge router with suitable example. **(10)**

Q.6 Explain constrained graph based compaction. **(10)**

OR

Q.6 Describe two dimensional compaction. **(10)**

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