S.D.E.

B.C.A. SEM – II (CBCS - 2018 Course) : SUMMER - 2019

SUBJECT : COMPUTER ORGANIZATION & ARCHITECTURE

Day : Thursday
Date : 02/05/2019

S-2019-4947

Time 10.00 AM TO 1.00 PM
Max. Marks : 70

N.B.

1) Attempt any **FOUR** questions from Section – I and any **TWO** questions from Section – II.
2) Answers to both the sections should be written in the SAME answer book.
3) Figures to the right indicate **FULL** marks.

SECTION – I

Q.1 What are combinational circuits? Explain the full-adder with circuit diagram. **(10)**

Q.2 Describe register transfer with the help of examples. **(10)**

Q.3 What is instruction cycle? Explain steps of instruction cycle with flow chart. **(10)**

Q.4 What is the need of cache memory? Discuss any two mapping techniques associated with cache memory. **(10)**

Q.5 Discuss various instruction formats with help of examples. **(10)**

Q.6 Write short notes on any **TWO** of the following: **(10)**

a) Input Output Processor
b) CISC
c) Assembly language

SECTION – II

Q.7 Convert the following numerical arithmetic expression into reverse polish notations and show the stack operation for evaluation of the numerical result. **(15)**

a) (3 + 4) [10 * (2+6) + 8]
b) (5 + 6) [(3+4) * (7-3)]

Q.8 Simplify the following Boolean functions using K-map. **(15)**

a) $F(x, y, z) = \sum(0, 2, 3, 4, 6)$
b) $F(A, B, C, D) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

Q.9 Draw the block diagram of Arithmetic logic shift unit and briefly describe its functioning with help of function table. **(15)**

* * *