B.Tech. SEM -VI Electronics 2014 Course (CBCS) : SUMMER - 2019
SUBJECT : VLSI DESIGN

Day : Monday
Date : 27/05/2019
S-2019-2745
Time : 02.30 PM TO 05.30 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat diagrams **WHEREVER** necessary.

Q.1 What is the need of attributes in VHDL? Describe any two attributes with example. **(10)**

OR

Q.1 Write VHDL code for 4- bit shift register for left shift and right shift. **(10)**

Q.2 What do you mean by metastability? What are the solutions? Explain any one in detail. **(10)**

OR

Q.2 Write VHDL code for 110 sequence detector using Moore machine. **(10)**

Q.3 Draw the architecture of FPGA. Describe the function of each block. **(10)**

OR

Q.3 Describe PLA structure with neat diagram and steps to implement Boolean function with example. **(10)**

Q.4 **a)** Describe structure of n-channel MOSFET with neat diagram. **(06)**

b) Write note on : source follower **(04)**

OR

Q.4 With the help of I-V characteristics derive expression for drain current. **(10)**

Q.5 Describe CMOS inverter characteristics. **(10)**

OR

Q.5 What is the significance of power delay product? A CMOS logic operates at $V_{DD} = 1V$, $f = 1GHz$ and load of 10pF. Calculate dynamic power dissipation. **(10)**

Q.6 Describe transmission gate. Design 4:1 mux using transmission gate. **(10)**

OR

Q.6 Implement two input NAND and AND gate using CMOS. **(10)**

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