B.Tech Sem – VII (2007 Course) (Electronics Engg.) : SUMMER - 2019

SUBJECT : VLSI DESIGN TECHNOLOGY

Day : Wednesday
Date : 15/05/2019

S-2019-3190

Time : 02.30 PM TO 05.30 PM
Max. Marks : 80

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in SAME answer book.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** What is test bench? Write test bench for a half adder. **[04]**

b) What is FSM? List its advantages and disadvantages. **[05]**

c) What is the function of 'hot plugging capability and slew rate control' in CPLD/FPGA? **[05]**

Q.2 **a)** Write VHDL code for 3:8 line decoder. **[06]**

b) Define attribute. List types of attributes. Describe any one in detail. **[07]**

Q.3 **a)** What do you mean by metastability? What are the solutions? Describe any one solution in detail. **[07]**

b) Design 110 sequence detector using Moore Machine. **[06]**

Q.4 **a)** Draw the architecture of CPLD XC 9500. Describe function block. **[07]**

b) Write note on : TAP controller. **[06]**

SECTION – II

Q.5 **a)** Describe the concept of two phase clocking. **[05]**

b) Write note on : BiCMOS Technology. **[05]**

c) What do you mean by technology scaling? What are the effects of technology scaling on chip level design? **[04]**

Q.6 **a)** Describe global routing and switch box routing. **[06]**

b) What are wire parasites? How do parasitics affect the performance of chip? **[07]**

Q.7 **a)** Describe CMOS inverter characteristics in detail. **[07]**

b) Describe 'body effect' in CMOS devices with neat diagram. **[06]**

Q.8 **a)** Design two input NAND gate using CMOS. **[07]**

b) Describe modularity with example. **[06]**

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