**B.Tech Sem – VI (2007 Course) (Computer Engg.) : SUMMER - 2019**
**SUBJECT: MICROPROCESSOR BASED SYSTEMS**

Day: Wednesday
Date: 29/05/2019

Time: 02.30 PM TO 05.30 PM
Max. Marks: 80

**S-2019-3115**

**N.B.:**

1) **Q. No. 1** and **Q. No. 5** are **COMPULSORY**. Out of the remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answer to both the sections should be written in **SAME** Answer book.
4) Use of non programmable **calculator** is **ALLOWED**.
5) Draw neat and labeled diagrams **WHEREVER** necessary.
6) Assume suitable data, if necessary.

## SECTION - I

| | | | |
|---|---|---|---|
| **Q.1** | **a)** | List the features of 80386. | **(05)** |
| | **b)** | State how granularity bit effects. | **(04)** |
| | **c)** | Draw and explain format of task state segment. | **(05)** |
| **Q.2** | **a)** | Explain different data types of 80386 in detail. | **(06)** |
| | **b)** | Describe addressing modes of 80386 with suitable example. | **(07)** |
| **Q.3** | **a)** | Explain the concept of segmentation in 80386. | **(06)** |
| | **b)** | Explain various fields in page directory entry and page table entry. State their functions. | **(07)** |
| **Q.4** | **a)** | Explain GDT, IDT and LDT. | **(06)** |
| | **b)** | Explain the nested task. | **(07)** |

## SECTION - II

| | | | |
|---|---|---|---|
| **Q.5** | **a)** | Differentiate between IDT and IVT. | **(04)** |
| | **b)** | Explain why dual core processors are well suited for multitasking environment. | **(04)** |
| | **c)** | Describe register bank of 8051 in detail. | **(06)** |
| **Q.6** | **a)** | Explain how interrupts and exceptions are handled in protected mode. | **(07)** |
| | **b)** | Explain interrupt handling in real mode. | **(06)** |
| **Q.7** | **a)** | Give specification of HP, Sony, Lenova laptop. | **(06)** |
| | **b)** | Explain PCI bus interface with neat diagram for single processor system. | **(07)** |
| **Q.8** | **a)** | Explain the operation of various timer modes of 8051 micro-controllers. | **(06)** |
| | **b)** | Explain any two SFRs of 8051 in detail and also define the concept of bit addressable and byte addressable. | **(07)** |

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