B. Tech. Sem – VIII (Biomedical Engg.) (2014 COURSE) (CBCS) : SUMMER - 2019

SUBECT: ELECTIVE-IV SYSTEM ON CHIP (SOC)

Day: Thursday
Date : 30/05/2019

Time: 02.30 PM TO 05.30 PM
Max. Marks: 60

S-2019-2942

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Assume suitable data if necessary.
4) Use of non-programmable **CALCULATOR** is allowed.

Q.1 **a)** Draw and explain SOC Design flow in brief. **(05)**

b) State the characteristics of typical deep submicron integrated circuit design illustrate the challenges facing SOC design teams. **(05)**

OR

Q.1 Describe in brief an Improved Design Methodology for SOC Design. **(10)**

Q.2 Explain the software structure in SOC design with necessary diagram. State the software trends. **(10)**

OR

Q.2 Describe the current SOC design flow with diagram. Also state the important incremental tool enhancements. **(10)**

Q.3 What are the basics of processor centric SOC architecture? Explain in brief with basic processor generation flow. **(10)**

OR

Q.3 Explain in detail the system design with Multiple Processors. **(10)**

Q.4 Explain Major decisions in Processor-Centric SOC Organization. **(10)**

OR

Q.4 Describe the following term in brief, **(10)**
"Communication Design= Software Mode + Hardware Interconnect"

Q.5 Describe in detail the pipelining for processor performance with simple RISC pipelines. **(10)**

OR

Q.5 What are the different methods used for optimizing processor to match hardware? **(10)**

Q.6 Explain following in brief, **(10)**

i) SOC and ROI (Return of Investment)
ii) The designers dilemma

OR

Q.6 Describe the limitations of general purpose processors and the SOC Design transition with respect to SOC. **(10)**

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