B. Tech. Sem - III (Computer Engg.) 2014 COURSE) (CBCS) :
SUMMER - 2019
SUBJECT: DIGITAL TECHNIQUES AND LOGIC DESIGN

Day : Monday
Date : 13/05/2019
S-2019-2558
Time : 02.30 PM TO 05.30 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 Simplify the following Boolean expressions using k-map and implement logic gates: **(10)**

$Y = \sum m\,(1, 2, 9, 10, 11, 14, 15)$

OR

State and prove De Morgan's theorem. Simplify following Boolean expression and realize using NAND gates only **(10)**

$Y = A + \bar{A}B + AB$

Q. 2 Distinguish between multiplexer and demultiplexer. Implement the following function using 8:1 Multiplexer. **(10)**

$F\,(A, B, C, D) = \sum m\,(0, 1, 3, 4, 8, 9, 15)$

OR

Describe two bit half adder and full adder with circuit diagram and truth table. How will you convert 4 bit binary adder to BCD adder. **(10)**

Q. 3 Describe working of S-R latch with neat circuit diagram and truth table. **(10)**

OR

Design and implement mod 5 counter. Draw timing diagram. **(10)**

Q. 4 Describe different types of Memory and their applications. **(10)**

OR

Describe the working of Bipolar Static RAM cell with neat diagram. Distinguish between SRAM and DRAM. **(10)**

Q. 5 What is PLA? Draw a combinational circuit for PLA with 3 inputs, three product terms and two outputs **(10)**

OR

Draw ASM chart and state diagram for a two bit down counter with output Q_1 and Q_0 and enable signal E. Design the circuit using JK flip flops. **(10)**

Q. 6 What is VHDL? Write entity and architecture declaration for two input AND gate and two input XOR gate. **(10)**

OR

Distinguish between sequential and concurrent execution of VHDL statements with suitable examples and execution flow. **(10)**

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