M. Tech.-I (Electronics V.L.S.I.) (CBCS – 2015 Course) : SUMMER– 2019

SUBJECT : DIGITAL VLSI DESIGN

Day : Saturday
Date : 18/05/2019

S-2019-3378

Time : 11.00 AM TO 02.00 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagrams **WHEREVER** necessary.
4) Assume suitable data if necessary.

SECTION - I

Q.1 What are the features of VHDL? How is it different from conventional programming languages? **[10]**

OR

Enlist and explain the basic data types and data objects in VHDL.

Q.2 Write VHDL code to implement tri-state buffer. **[10]**

OR

Write VHDL code to implement an 8 input priority encoder.

Q.3 What is the concept of "test-bench" ? Explain with an appropriate example. **[10]**

OR

Write VHDL code for synchronous D-Flip Flop using "IF" construct.

SECTION – II

Q.4 Explain synthesis flow in detail. Why is logic optimization required for synthesis? **[10]**

OR

What is the importance of "Floor Planning" process? How does it affect the performance of the design?

Q.5 Explain the "LUT" with neat diagrams. How is a logic function implemented using LUT? **[10]**

OR

Explain the terms "Parallel Expanders" and "Shareable Expanders" with respect to CPLD.

Q.6 Implement the logic function Y=AB+C using multiplexer. **[10]**

OR

Implement the logic function Y=AB+C using LUT (Assume LUT uses transmission gates)

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