B.Tech Sem - III (2007 Course) (Computer Engg.) : SUMMER - 2019
SUBJECT: DIGITAL LOGIC TECHNIQUES

Day : Monday
Date : 13/05/2019

Time 02.30 PM TO 05.30 PM
Max. Marks: 80

S-2019-2972

N. B. :

1) **Q. No.1** and **Q. No. 5** are **COMPULSORY**. Out of remaining attempt **Any TWO** questions from each section.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the 'SAME' answer book.
4) Neat diagrams must be drawn **WHEREVER** necessary.

SECTION-I

Q.1 **a)** Carry out following conversions. **(06)**

i) $(193)_{16} = (\quad)_8$
ii) $(49.25)_{10} = (\quad)_2$
iii) $(1010101)_2 = (\quad)_{10}$

b) State advantages of CMOS devices over TTL devices. **(04)**
c) What is function of Shift Register? State its applications. **(04)**

Q.2 **a)** Simplify following function using K map and implement using logic gates. **(07)**
$Y = \sum m\,(1,3,7,11,15) + d\,(0,2,5)$
b) State and prove De Morgan's theorem with the help of truth table and logic design. **(06)**

Q.3 **a)** Describe the operation of TTL NAND gate with the help of neat circuit diagram. **(07)**
b) Design parity generator using basic gates to produce digital word with odd parity. **(06)**

Q.4 **a)** Draw neat diagram of JK flip flop using SR Flip flop. Write truth table and explain working. **(07)**
b) What is MOD counter? Design Mod -5 Asynchronous counter using JK flip flop **(06)**

SECTION-II

Q.5 **a)** Distinguish between Static and Dynamic RAM **(06)**
b) Describe the general form of Moore circuit with example **(04)**
c) Draw and explain general structure of PLA. **(04)**

Q.6 **a)** Describe the working of Bipolar static RAM cell with neat diagram. **(07)**
b) Describe the structure and programming of EPROM with neat diagram. **(06)**

Q.7 **a)** Design a sequence detector to detect three or more consecutive "1"s in a sting of input bits. **(07)**
b) Draw state diagram and write State table and State equation for clocked D flip flop. **(06)**

Q.8 **a)** What is VHDL? Write VHDL code using structural modeling for SR Latch using NAND gates. **(07)**
b) Draw ASM chart for sequential circuit with control input E and counts up from 0 to 3. **(06)**

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