B.Tech. SEM -IV Info. Tech. 2014 Course (CBCS) : SUMMER - 2019
SUBJECT: DIGITAL ELECTRONICS AND LOGIC DESIGN

Day: Tuesday
Date: 28/05/2019

Time: 10.00 AM TO 01.00 PM
Max Marks: 60

S-2019-2619

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw diagrams **WHEREVER** necessary.

Q.1	List and explain characteristics of digital IC's.	**(10)**
	OR	
Q.1	Compare and discuss characteristics of TTL and CMOS.	**(10)**
Q.2	Simplify using Quine McCluskey method $F= \sum (0,1,2,3,5,7,8,9,11,14)$	**(10)**
	OR	
Q.2	Explain k map representation of logic functions with suitable example.	**(10)**
Q.3	Explain 3-bit ripple or asynchronous counter in detail.	**(10)**
	OR	
Q.3	Explain D and T flip flops in detail.	**(10)**
Q.4	Explain Moore machine representation.	**(10)**
	OR	
Q.4	Draw state diagram of different flip flops.	**(10)**
Q.5	Explain content addressable memory with suitable example.	**(10)**
	OR	
Q.5	Describe DDR and QDR SRAM with its advantages and disadvantages.	**(10)**
Q.6	Demonstrate design of simple controller.	**(10)**
	OR	
Q.6	Discuss VHDL modeling styles.	**(10)**

* * * * *