B.Tech Sem – V (2007 Course) (Computer Engg.) : SUMMER - 2019

SUBJECT : COMPUTER ORGANIZATION

Day : Tuesday
Date : 14/05/2019

Time 10.00 AM TO 01.00 PM
Max. Marks : 80

S-2019-3065

N. B. :

1) **Q. No. 1** and **Q. No. 5** are **COMPULSORY**. Out of remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the SAME answer books.
4) Draw neat and labeled diagram **WHEREVER** necessary.
5) Assume suitable data, if necessary.

SECTION - I

Q. 1 **a)** Draw and explain Von-Neumann architecture. **(06)**

b) Illustrate the procedure to calculate the 2's complement. **(04)**

c) Explain instruction pipelining in 80386 **(04)**

Q. 2 **a)** Describe instruction cycle in detail. **(06)**

b) List and explain addressing modes of IBM 360 with suitable example. **(07)**

Q. 3 **a)** Explain non-restoring method of division. **(07)**

b) Draw the flow chart to explain how floating point addition is performed. **(06)**

Q. 4 **a)** Explain 80386 architecture with neat diagram. **(07)**

b) Explain the significance of control register and debug register of 80386. **(06)**

SECTION – II

Q. 5 **a)** Explain replacement algorithms for cache memory. **(06)**

b) Explain the format of micro-instruction. **(04)**

c) Explain the function of bus controller. **(04)**

Q. 6 **a)** Explain combinational and sequential ALU with neat diagram. **(06)**

b) Describe micro-instruction sequencing for the micro-instruction format with single address field. **(07)**

Q. 7 **a)** Explain the process of recording and retrieving data from CDROM. **(06)**
b) Explain DRAM with its performance characteristics. **(07)**

Q. 8 **a)** Explain inter-processor communication between CPU and co-processor. **(07)**
b) Explain the concept of RISC architecture with neat diagram. **(06)**

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