M.Tech. Electronics-III Self Study-I

MISORI – III (2015 COURSE) (CBCS): WINTER – 2016
SUBJECT : SELF-STUDY PAPER – I: IN-VEHICLE NETWORKING

Day : Monday
Date : 19/12/2016

Time : 11.00 AM TO 02.00 PM
Max. Marks : 60

N.B.:

1) All questions are **COMPLOSRY**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer books.

SECTION – I

Q.1 Explain different layers of OSI reference model. **[10]**

OR

Explain the following with reference to vehicle networking:
a) Data communication b) Networking

Q.2 Write a note on RARP. **[10]**

OR

Compare Ethernet, TCP and IP.

Q.3 Explain in detail the message frame of CAN protocol. **[10]**

OR

Write a note on CAN open-device net.

SECTION – II

Q.4 What is the concept of LIN? Justify its role in automation. **[10]**

OR

Compare CAN and LIN protocol.

Q.5 What is the role of MOST in networking? Give the details of application also. **[10]**

OR

Which topology is used in Flex Ray? Explain in detail.

Q.6 What is meant by positioning? Explain importance of GPRS in vehicle networking. **[10]**

OR

What is the concept of latitude while defining the GRID system? Discuss.

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MISORI-III (CBCS-2015 COURSE): WINTER-2016
SUBJECT: SELF- STUDY PAPER-I IC FABRICATION TECHNOLOGY

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4) Draw neat and labeled diagram **WHEREVER** necessary.
5) Assume suitable data, if necessary.

SECTION-I

Q.1 Describe diffusion and ion implantation. **(10)**

OR

Describe RCA wafer cleaning technique. **(10)**

Q.2 Describe thermal oxidation in detail. **(10)**

OR

List the properties of oxide layer on silicon and describe oxidation of silicon. **(10)**

Q.3 Describe the process of photolithography in detail. **(10)**

OR

Describe electron beam lithography in detail. **(10)**

SECTION-II

Q.4 Describe low pressure CVD reactor. **(10)**

OR

Describe laser enhanced CVD. **(10)**

Q.5 Describe failure mechanism in interconnects. How can it be avoided? **(10)**

OR

Describe gas flow sputtering deposition method. **(10)**

Q.6 Describe rapid thermal CVD. **(10)**

OR

Describe plasma enhanced CVD. **(10)**

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MISORI – III (CBCS – 2015 COURSE) : WINTER - 2016
SUBJECT: SELF STUDY PAPER – II h) LOW POWER VLSI DESIGN

Day: Monday
Date: 19/12/2016

Time: 11.00 AM TO 02.00 PM
Max Marks. 60

N.B.

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SECTION - I

Q.1 With suitable diagram discuss MOS modeling. **(10)**

OR

Discuss the physics of power dissipation in CMOS devices. **(10)**

Q.2 Which are the major sources of power dissipation in digital ICs? **(10)**

OR

Discuss static power dissipation. **(10)**

Q.3 Explain low power techniques at device level. **(10)**

OR

Describe low power techniques at circuit level. **(10)**

SECTION - II

Q.4 Discuss low power digital cells. **(10)**

OR

How switching activities can be reduced? **(10)**

Q.5 What is Dual V_T? How it helps in low power operation? **(10)**

OR

How transistor stacking helps in obtaining low power? Discuss in detail. **(10)**

Q.6 Describe zero skew v/s tolerable skew. **(10)**

OR

Explain power dissipation in clock distribution. **(10)**

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MISORI-III (CBCS 2015 COURSE): WINTER- 2016

SUBJECT: ELECTIVE-I: PROGRAMMABLE SYSTEM ON CHIP

Day: Wednesday Time: 11.00 A.M. To 2.00 P.M.

Date: 14-12-2016 Max Marks: 60

N.B:

1) All questions are **COMPULSORY.**
2) Both the sections should be written in **SEPARATE** answer book.
3) Figures to the right indicate **FULL** marks.
4) Neat diagrams must be drawn **WHEREVER** necessary.

SECTION-I

Q.1 What is difference between system on chip (SOC) and programmable system on chip (PSoC). **(10)**

OR

Write the difference between PSoC3 and PSoC5.

Q.2 Explain in detail CPU Sub System. **(10)**

OR

Explain in detail IO Sub System.

Q.3 Explain the Memory Management in PSoC. **(10)**

OR

What are the fixed functions available in PSoC. Explain any one in detail.

SECTION-II

Q.4 Write a program to display message on LCD using PSoC controller. Write all steps involved for the same in PSoC creator. **(10)**

OR

Write a program for implementation of Volt Meter in PSoC. Also draw the block diagram.

Q.5 Explain in detail Delta Sigma ADC. In which family of PSoC of Delta Sigma ADC is available. **(10)**

OR

Draw the interface diagram for Stepper Motor interface with PSoC. Draw the flow chart for the software.

Q.6 Explain the following: **(10)**

a) Boundary scan
b) JTAG Interface

OR

a) Interrupt Controller in PSoC
b) Driving modes of IOs in PSoC

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MISORI – III (CBCS – 2015 COURSE) : WINTER – 2016
SUBJECT : ELECTIVE – 2 : TESTING AND VERIFICATION OF VLSI DESIGN

Day : Friday
Date : 16-12-2016

Time : 11.00 A.M. To 2.00 P.M.
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
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4) Assume suitable data, if necessary.

SECTION - I

Q. 1 Define verification. How human factor plays role in verification? How to reduce it? **(10)**

OR

How formal verification is performed? Discuss with suitable reconvergence model. **(10)**

Q. 2 What is the purpose of verification tools? Discuss linking tools. **(10)**

OR

How simulator plays a role in verification? Describe its types with suitable example. **(10)**

Q. 3 How system and board level verification is performed? Describe with suitable example. **(10)**

OR

What are the component and system level features? Explain with respect to verification. **(10)**

SECTION – II

Q. 4 What is Testing? Why Testing is required? Which are the possible faults in digital circuit? **(10)**

OR

Discuss fault detection and fault dominance. **(10)**

Q. 5 How testable combinational logic circuits are designed? **(10)**

OR

Describe in brief: Test generation for sequential circuits. **(10)**

Q. 6 What is DFT? How it is beneficial in testing? **(10)**

OR

Describe BIST with suitable diagram. **(10)**

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